## REMARKS

This paper is being provided as a supplement to Applicant's response filed on May 6, 2003, and is a response to the Office Action dated February 11, 2003, for the above-captioned U.S. patent application. In this response, claims 1-14 and 16-18 have been cancelled and claims 19-28 have been added to clarify that which Applicant considers to be the invention. Applicant respectfully submits that the amendments to the claims and the new claims are fully supported by the originally filed specification.

Applicant thanks the Examiner for the allowance of Claim 15.

Applicant has added new claims 19-28 and respectfully submits that these claims are allowable over the prior art of record.

U.S. Patent No. 4,970,694 to Tanaka (hereinafter "Tanaka") discloses supplying a first chip enable signal for determining the operation timing of a memory chip to a first chip enable input circuit. Tanaka's Figure 7 discloses a first chip enable input circuit 1 that includes CMOS inverters 31-39, MOS capacitors 40-42 and CMOS NAND gate 43. Signal CE1 is supplied to one input terminal of the NAND gate 43 via inverters 31 to 33 The output of inverter 33 is supplied to the other input terminal of the NAND gate 43 via delay circuit 30 formed of inverters 34 and 36 and capacitors 40 to 42. The output of NAND gate 43 is supplied to a second chip enable circuit 2 via inverters 37 to 39. (Col. 3, Line 60-Col. 2, Line 3; Figure 7).

Applicant respectfully submits that the delay circuit 30 of the Tanaka citation does not generate a delay signal according to the present invention. Applicant refers the Examiner to

Exhibit 1, submitted herewith, in which waveforms in the delay circuit 30 of Figure 7 of Tanaka are shown along with the waveforms in the circuits of Applicant's Figures 4 and 6 of the present application. In Tanaka's delay circuit 30, the output level of the inverter 3-4 changes immediately in response to the rise-edge of the output signal of the inverter 33 (corresponding to the logic signal in the present invention) and the output level of the NAND gate 43 changes immediately in response to the output of the inverter 36. The capacitors 40-42 in the delay circuit 30 are provided not to set a delay time of the rise-edge of the output signal of the inverter 33 but rather to set the width of the output signal of the NAND gate 43. This is to say, the delay circuit 30 does not intend that the output of the NAND gate 43 changes late according to the delay of the rise-edge of the output of the inverter 33 due to the capacitors 40-42.

Moreover, there are no descriptions about the channel type of the capacitors 40-42 in Tanaka. Therefore, assuming that the inverters 40-42 are n-type and the inverter 41 is p-type similarly to Applicant's Fig. 1A of the present application based on the descriptions about Vss and Vdd of the delay circuit 30 in Tanaka's Fig. 7, a meaningful change of the output of the inverter 33 for making the NAND gate 43 to output one shot pulse is a rise-edge. In that case, the outputs of the inverters 34 and 36 rise up and the output of the inverter 35 falls down. As a result, the capacitance of each capacitor decreases. In other words, each capacitor operates so as not to affect the delay of the signal, which is different from the concept of the present invention.

In light of the above, Applicants respectfully submit that Tanaka does not teach or suggest the technical concept of the present invention. In the first place, Tanaka does not recognize the problems to be solved by the present invention, and, secondly, it does not provide the motivation to create the present invention.

U.S. Patent No. 5,459,424 to Hittori (hereinafter "Hittori") discloses only that both an n-MOS capacitor and a p-MOS capacitor are provided at the same node, as seen in Figure 1.

U.S. Patent No. 6,040,713 to Porter et al. (hereinafter "Porter") discloses only that same-type MOS capacitors are provided at all nodes, as seen in Figure 11.

On the other hand, in Applicant's new claim 19, the node coupled to the MOS capacitor of the first channel type is different from the node coupled to the MOS capacitor of the second channel type. Such configuration is not disclosed nor suggested in any of the prior art of record.

In Applicant's new claim 22, the same-type MOS capacitors are coupled to the nodes alternately. If such a configuration is not used, it is impossible to widely delay only one of the rise-edge and the fall-edge.

Applicant's new claims 25-28 recite configurations of the embodiments (Figs. 4 and 6) implementing the concepts of the present invention, which are not taught or suggested in any of the prior art of record.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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Fig. 7 in Tanaka citation

waveform in delay circuit 30

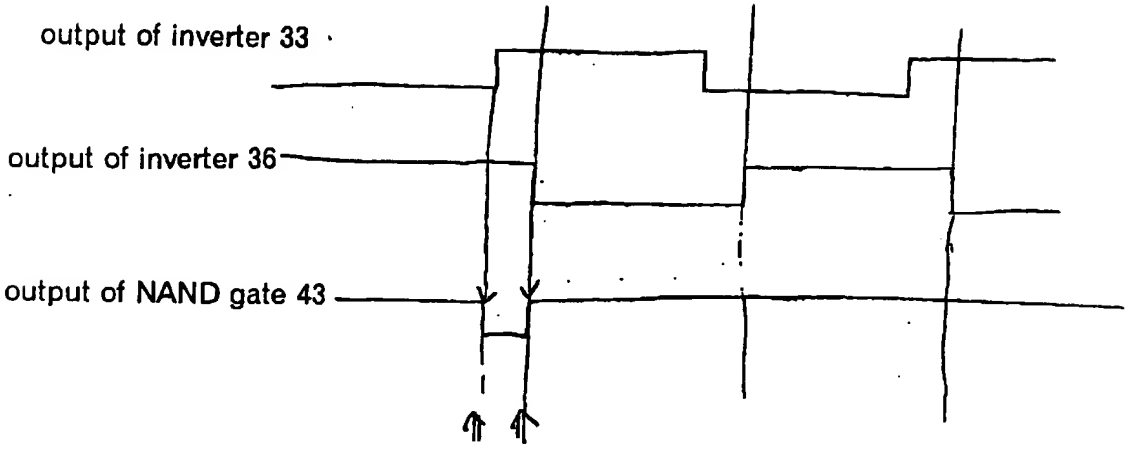


Fig. 4 in the present application

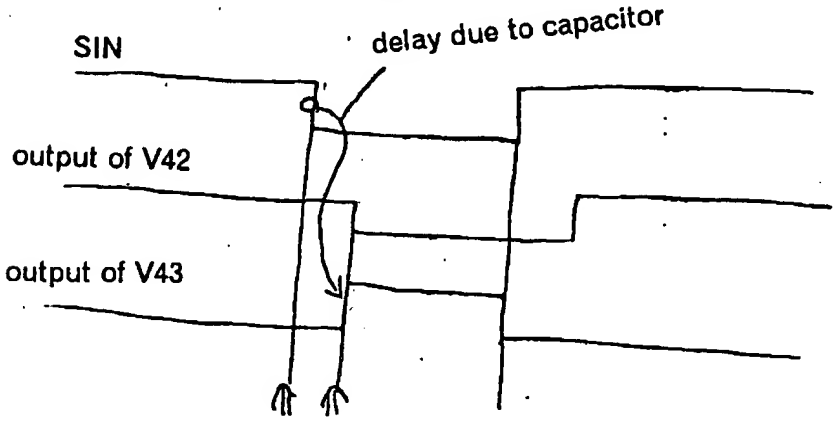


Fig. 6 in the present application

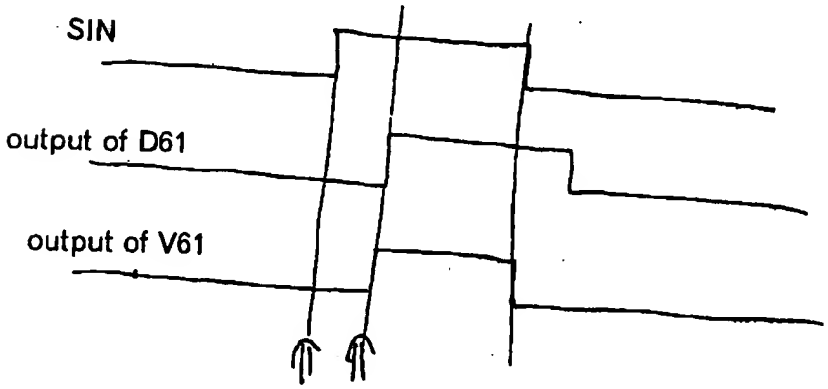


EXHIBIT 1

TITLE: DELAY CIRCUIT AND METHOD
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Sheet 1 of 1 Docket No. SIM-01501